Patent #10

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Luan Tran Et Al.	Group Art Unit:	2815
Serial No.:	10/059,727	Examiner:	Jesse A. Fenty
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For:	Memory Cell Arrays	Atty. Dkt. No.:	MCT.0004C1US (97-0903.02)

Commissioner for Patents
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APPEAL BRIEF

Sir:

Applicant respectfully appeals from the final rejection mailed June 18, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., the assignee of the present application by virtue of the assignment recorded at Reel/Frame 010585/0369.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

Claims 1-8 and 10-25 have been finally rejected and are the subject of this appeal. Claim 9 was rejected under the judicially created doctrine of obviousness-type double patenting over U.S. Patent No. 6,410,948 in view of U.S. Patent No. 5,107,459. A terminal disclaimer was timely filed on August 18, 2003 to obviate the double patenting rejection. In the Advisory Action dated October 1, 2003, claim 9 was objected to, but not rejected. The Amendment Under

Date of Deposit: 11/18/2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313.
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37 C.F.R. § 1.116 submitted herewith amends claim 9 from dependent form to independent form, with the scope of claim 9 remaining unchanged. Therefore, claim 9 should be allowed.

IV. STATUS OF AMENDMENTS

An Amendment after final (Amendment Under 37 C.F.R. § 1.116) is submitted herewith. In the Amendment, claim 9 has been amended into independent form. The only rejection of claim 9 was an obviousness-type double patenting rejection, which has been obviated by the timely filed terminal disclaimer on August 18, 2003. This Amendment reduces the issues for appeal (by removing the objection of claim 9) and thus should be entered.

V. SUMMARY OF THE INVENTION

Fig. 1A is a schematic diagram of an exemplary memory array 20 in a memory device that includes word lines 26 running generally in parallel along one direction and bit line pairs 32 running generally in parallel along a perpendicular direction. A memory cell is represented schematically as a capacitor 8, and is connected by a transistor 9 to one of the bit lines BL. Each transistor 9 is activated by a word line 26. Specification, p. 4, ¶ [0034].

A row of memory cells 8 is selected upon activation of a word line 26. The state of each memory cell in the row is transferred to a bit line 32 for sensing by the sense amplifiers 35, each connected to a pair of bit lines 32. In the illustrated embodiment, the bit lines 32 are vertically twisted at one or more predetermined locations in the array 20 to reduce soft error rates. Specification, p. 4, ¶ [0035].

Fig. 2A shows the layout of a portion of the memory array of a semiconductor memory device according to one embodiment (which may be a dynamic random access memory or DRAM, for example). Other types of memory devices include synchronous DRAMs, video

RAMs, or other modified versions of the DRAM. The memory array 20 includes a semiconductive substrate 22. Specification, p. 4, ¶ [0036].

The memory cell transfer transistors 9 are formed in the substrate 22 in a plurality of continuous active areas 24 running generally in parallel to each other. Each active area 24 is defined between isolation regions 34 (see Fig. 3) disposed relative to the substrate 22. To form a transistor in an active area, impurity doped regions (not shown) are formed in the substrate (along the length of each active area 24) to create the source and drain of the transistor. A word line 26 forms the gate of the transistor. Specification, p. 5, ¶ [0037]

The transistor formed in the active area provides the pass gate that is controllable to electrically connect a cell capacitor (indicated as 102A, B, C, or D in Fig. 2A) to a bit line 32. Each of the capacitors 102 is electrically connected by contact plugs to an active area line 24 portion forming a node (source or drain) of a transistor 9. Each bit line 32 is connected to the active area line portion forming the other node of the transistor 9 by bit contact 100A or 100B. For example, activation of a word line 26C will cause the stored charges from the capacitors 102A and 102B to be transferred by corresponding transistors 9 to bit lines 32. Although depicted as squares in Fig. 2A, the contacts 100 can be of different shapes, and can take up the entire area of intersection between the bit lines 32 and the active area lines 24. Specification, p. 5, ¶ [0038].

For clarity, each illustrated continuous active area line 24 has been shown to extend to outside of the boundary of substrate 22 utilizing dashed lines. Each individual active area is designated separately as 24', 24", and 24"'. To reduce the effective memory cell area while still maintaining ease of manufacture as discussed below, the continuous active areas 24', 24", and 24"' are not straight or linear, but rather weave relative to the substrate within which they are

formed such that bends are created in each active area line 24 as it extends across the array. Effectively, the active area lines appear wavy across the array. The illustrated individual continuous active area lines extend generally horizontally across the page upon which Fig. 2A appears, but jog upwardly repeatedly as depicted in Fig. 2A to form protruding portions 19. This jogging is repeated along the length of the active area line 24. Specification, p. 5, ¶ [0039].

Similarly, the bit lines 32 (which are formed above the active area lines 24) also weave relative to the substrate such that repeated depressed portions 21 are formed in the bit lines. The bit lines 32 run generally along the same direction as the active areas 24, but the direction of the jog in the bit lines 32 is opposite to the jog of the active area lines 24. Thus, in the Fig. 2A embodiment, both bit lines and active area lines are formed to be wavy as they extend generally across the memory array. The bit lines and active area lines intersect at slanted portions 17 and 15, respectively, where the bit lines and active area lines are bent. In the Fig. 2A embodiment as well as in some other embodiments such as those described below, corresponding edges of the bit lines and active area lines are laterally spaced apart by some distance, that is, the bit lines and active area lines do not extend completely one on top of another except where they intersect at slanted portions. Specification, p. 5, ¶ [0040].¶

Bit contacts 100 are formed at the intersections of the bit lines 32 and the active area lines 24. Since the bit lines 32 and active area lines 24 are slanted with respect to each other in the region of each intersection, formation of the contact hole in which the bit contact 100 is formed is made easier. This is because of the increase in width W of the contact hole (such as the contact hole 40 in Fig. 5) as compared to the width if both the active area lines 24 and bit lines 32 are generally straight. As the feature size of memory devices continue to decrease (e.g., 0.18

or 0.25 microns), such increases in the width of the bit contact holes result in generally more reliable bit contacts. Specification, p. 6, ¶ [0041].

More specifically, as depicted in Fig. 2A, each of the bit lines 32 and active area lines 24 run generally along the X direction. The jogs in the bit lines and active area lines are formed at predetermined positions A-A, B-B, C-C, and D-D. At position A-A, each active area line 24 bends or jogs in a first direction (e.g., upwards) while each bit line 32 bends or jogs in a second, opposite direction (e.g., downwards). The angle of the bends can be set at, for example, about 22.5°, although other angles are also possible. In addition, the directions of the active area and bit lines bends or jogs can be switched. Specification, p. 6, ¶ [0042].

As further shown in Fig. 2A, at position B-B, each of the active area and bit lines bends or jogs back in the opposite directions of the corresponding bends or jogs at position A-A such that both the active area and bit lines run again generally along the X direction. At position C-C the active area and bit lines bend or jog again, also in the opposite directions from the corresponding bends or jogs at position A-A. At position D-D, the lines bend or jog back to run generally in the X direction. Specification, p. 6, ¶ [0043].

One advantage of weaving both the active area and bit lines in the array is that a smaller bend angle is required for the repeated jogs while still achieving the desired memory cell area reduction. Specification, p. 7, ¶ [0044].

Further, if desired, the amount of bending of the active area and bit lines can be selected to be different. Thus, for example, the angle of the bends in each active area line can be selected to be larger than the angle of the bends in each bit line. This may be desirable since it is easier to form the deeper jogs in the active area lines since they are formed in a relatively flat surface of

the substrate as compared to the bit lines, which are formed over a number of structures, including word lines. Specification, p. 7, ¶ [0045].

A plurality of conductive lines 26, 28 are also formed (under the bit lines 32) that run generally perpendicularly to the active area 24 and bit lines 32. In the illustrated example, four of the conductive lines are designated with numeral 26 and one of the conductive lines is designated with numeral 28. A pair of conductive lines 26 may be seen on either side of conductive line 28. The conductive lines 26 form the access or word lines (or access gates) in the DRAM array, while the conductive lines 28 are grounded to provide isolation lines (or isolation gates) between word lines 26. Conductive lines 26, 28 run generally vertically as viewed in Fig. 2A. The active area lines 24 and conductive lines 26, 28 constitute or define an array over which a plurality of memory cells are formed. Specification, p. 6, ¶ [0046].

In the array 20, the word or access lines 26 are relatively straight (formed generally as parallelograms in given portions of the array). The word or access lines 26 intersect slanted portions of the active area lines 24 and bit lines 32. Specification, p. 7, ¶ [0047].

The area which is consumed by a single memory cell in accordance with this embodiment is illustrated by dashed outline 30. Such area can be considered or described as relative to the feature size F, as discussed above. As shown, a single memory cell is about 3F wide by about 2F deep, thus providing a consumed area for a single memory cell of about $6F^2$. In one implementation, F is no greater than 0.25 micrometer, and preferably, no greater than 0.18 micrometer. However, other dimensions (either larger or smaller) are also contemplated. Specification, p. 7, ¶ [0048].

In one implementation, adjacent word lines 26 share an intervening bit contact 100 of adjacent pairs of memory cells as will become apparent below. For example, as shown in Fig.

2A, word lines 26C and 26D share bit contacts 100A and 100B, while word lines 26A and 26B share bit contacts 100C and 100D. Electrical isolation between the adjacent pairs of memory cells is provided by intervening isolation line 28. Line 28, in operation, is connected with a ground or suitable negative voltage. Alternatively, the electrical isolation can be provided by field oxide. Specification, p. 8, ¶ [0049].

Bit contacts 100, which can be formed of an electrically conductive plug 46 (as shown in Fig. 12) and can be made of a conductively doped polysilicon, electrically connect the bit lines 32 to the underlying active areas 24. The bit contacts 100 are located in the space 104 between two adjacent word lines 26. The memory cell capacitors 102 are electrically contacted to the active areas 24. Specification, p. 8, ¶ [0050].

The Fig. 2B embodiment is the same as the Fig. 2A embodiment except that bit contacts 101 (101A, 101B, 101C, and 101D illustrated) in the Fig. 2B embodiment are formed with a different process than bit contacts 100 (100A, 100B, 100C, and 100D) in the Fig. 2A embodiment. Similarly, formation of contacts from electrodes of capacitors 102 to corresponding active areas 24 is also different. This is described further below. Specification, p. 8, ¶ [0051].

According to one embodiment, cross-sectional views of the memory array 20 of Fig. 2A are shown in Figs. 12 and 19A, which are cross-sections taken along lines 12-12 and 19-19, respectively. In Fig. 12, active areas 24 are defined relative to the substrate 22, with the bit contacts 100, which include electrically conductive plugs 46, disposed above and in electrical contact with portions of the active areas 24. Further, the bit lines 32, which can be formed of electrically conductive multilayer structures 56, are disposed above and in electrical contact with the bit line contact plugs 46. Specification, p. 8, ¶ [0052].

In Fig. 19A, the cell capacitors 102 are illustrated. Fig. 19B illustrates an alternative embodiment, as described below. Each capacitor 102 is formed of a first capacitor plate 64, a dielectric layer 66, and a second capacitor plate 68. The first capacitor plate 64 of each cell is electrically contacted to the plug 46 for electrical connection to the active area 24. The cell capacitor structure is laid over the bit line structure 56, which forms a cell-over-bit line (COB) array structure. An advantage the COB structure offers is that bit line contact openings need not be made in the second capacitor plate 68, which eliminates difficulties associated with aligning bit line contact openings in the second plate 68 to cell structures or word lines in the array. The bit line structure 56 is referred to as a buried bit line and corresponds to the bit line 32 in Fig. 2A. Specification, p. 8, ¶ [0053].

Although Figs. 12 and 19A illustrate details of cross-sections of the memory array according to one embodiment, it is to be understood that the invention is not to be limited in this respect. Other types of memory structures are contemplated and within the scope of the present invention. Specification, p. 9, ¶ [0054].

In the illustrated embodiment, a "double deck" bit line architecture is used, which includes the buried bit line 56 and a top deck bit line 33 (Figs. 12 and 19A) formed above the buried bit lines 32 and the capacitors 102. As shown in Figs. 12 and 19A, an insulating layer 39 is formed between the top deck bit line 33 and the underlying structure. The top deck bit line 33 is generally formed of a metal, such as aluminum. In Fig. 1A, the top deck bit line 33 is represented schematically as solid lines, while the buried bit lines 32 are represented as dashed lines. The top deck bit lines 33 do not make contact with the memory array. Contact to the memory array transistors are made by the buried bit lines. At the locations where twists are indicated (such as vertical twists 29 and 31 in Fig. 1A), the top deck bit line 33 is connected to a

buried bit line 32. Because the top deck bit lines 33 do not need to make contact to the underlying cell structure, they can be relatively straight, as shown in Figs. 12 and 19A. In addition, contact openings are not needed through the second capacitor plate 68 (Fig. 19A) of the memory array. This avoids problems associated with aligning the contact openings in the second capacitor plate 68 to the underlying word line and bit line structures. Specification, p. 9, ¶ [0055].

By using the double deck bit line structure, the bit lines 32, 33 can be connected to the sense amplifiers 35 in a vertically folded bit line configuration, as depicted in Fig. 1A. Thus, with the double deck bit lines in a vertically folded bit line arrangement, the column pitch occupies a 2F width, as opposed to a 4F pitch for traditional memory cells. This allows formation of a $6F^2$ memory cell. One advantage of the folded bit line configuration is that it is less susceptible to soft errors than the open bit line configuration. Because a bit line pair is connected to each sense amplifier 35 on the same side of the sense amplifier, noise created by alpha particles will couple to both of the bit lines in the pair. As the sense amplifier 35 detects the difference in voltage between the pair of bit lines, errors due to such noise effects are reduced. In an alternative embodiment, the $6F^2$ memory cell may be used with an open bit line arrangement, in which BL and BL_ are on opposite sides of a sense amplifier, as illustrated in Fig. 1B. Specification, p. 9, ¶ [0056].

Referring to Fig. 21, an alternative embodiment of an array containing reduced size memory cells (e.g., $6F^2$ cells) is shown. In this configuration, bit lines 200 are formed to weave relative to the substrate 20, while continuous active area lines 202 are generally straight. Bit contacts 206 are formed at the intersections between the bit lines 200 and active area lines 202. In addition, memory cell capacitors 208 are formed over and are in electrical contact with

portions of the active area lines 202. Although illustrated as generally straight it is to be understood that the straightness of the active area line or other structures (including bit lines) in this application depends on manufacturing tolerances. In addition, slight protrusions may be needed for forming contacts or other structures. Specification, p. 10, ¶ [0057].

As illustrated, each bit line 200 runs generally in the X direction and jogs or protrudes upwardly in a repeated pattern. Each bit line 200 bends upwardly at position A-A (at an angle of about 45° with respect to the X axis). The bit line 200 then bends in the opposite direction at position B-B so that it runs generally in the X direction. After a short run, the bit line 200 then bends downwardly at position C-C. At position D-D, the bit line 200 again bends back to run generally in the X direction. This pattern is repeated throughout the memory array to provide a wavy bit line. Specification, p. 10, ¶ [0058].

As indicated by the dashed outline 210, the feature size of the memory cell in this configuration is also about $6F^2$ (3F by 2F). Conductive lines 204, 205 run generally perpendicularly to the active areas 202. The conductive lines 204 form the word lines in the array while the lines 205 are grounded or driven to a negative voltage to provide electrical isolation between word lines 204. Specification, p. 10, ¶ [0059].

In comparing the memory cell layouts shown in Figs. 2A and 21, one advantage offered by the cell layout of Fig. 2A is that photolithography exposure to form the bit lines and active areas is easier to achieve due to the smaller bends of the bit lines and active areas in the Fig. 2A embodiment. Specification, p. 11, ¶ [0060].

Referring to Fig. 22, an alternative memory cell configuration is illustrated. In this configuration, the bit lines 300 are generally straight while the active area lines 302 weave relative to the bit lines. In this embodiment, the continuous active areas 302 run generally in the

X direction and have repeated downward jogs. Creating weaving continuous active areas can be simpler than creating weaving bit lines. Active areas are defined by isolation regions relative to a substrate, which initially is on a flat surface of a wafer. Because of the flatness, the bends in the active areas do not create as many photolithographic difficulties as with bit lines, which generally run over relatively rough terrain since the bit lines make contact to the active area surface in some portions and are isolated from active areas in other portions (where the cell capacitors are formed). Specification, p. 11, ¶ [0061].

At position A-A, the active area lines 302 bend at an angle of about 45°, then bend back at position B-B to run in the X direction. At position C-C, the active area lines bend in the opposite direction from the A-A bend, and bend back to run in the X direction again at position D-D. This pattern is repeated throughout the array. Specification, p. 11, ¶ [0062].

Bit line contacts 306 are defined at the intersection regions of the bit lines 300 and active areas 302, and memory cell capacitors 310 are formed over portions of the active area 302 for connection to the bit lines in response to activation of a word line. Again, the effective memory cell area is $6F^2$, as indicated by the dashed outline 310. Specification, p. 11, ¶ [0063].

Referring to Fig. 23, a staggered, weaving bit line configuration is illustrated. In this configuration, continuous active area lines 402 are straight while bit lines 400 (which run generally in the X direction) are bent at predefined positions. The bit lines 400 are staggered because they continue to bend in the same direction and do not bend back as in the configuration of Fig. 22. At position A-A, the bit lines 400 bend in a first direction by about 45°, then bend back at position B-B to run in the X direction. At position C-C, the bit lines 400 bend again in the first direction, and bend back at position D-D. This is repeated throughout the array. Because the bit lines are so staggered, the entire array needs to be staggered to accommodate the

generally diagonal direction of a column in the array. As a result, the array ends up being generally trapezoidally shaped. Specification, p. 11, ¶ [0064].

Running generally perpendicularly to the active area lines 402 are conductive lines 404, 405. The conductive lines 404 are word lines, while the conductive line 405 is grounded or negatively biased to provide isolation. Specification, p. 12, ¶ [0065].

Thus, in the embodiments described, either the bit lines or active area lines, or both, may be weaved by bending the lines at predetermined locations. As examples, the bends in the bit lines and active area lines may range between about 15° and 60°, although larger or smaller angles may be possible with other embodiments. Specification, p. 12, ¶ [0066].

Embodiments of the invention may have one or more of the following advantages. The memory array size can be reduced while not significantly increasing the complexity of the fabrication process. Ease of contact from the bit lines to a node in the memory cell is maintained even though memory cell size is reduced. The cell provides a larger area for the capacitor container, thereby reducing the stack height and the vertical height of the bit line contact. No contacts are necessary in the memory array, thereby making contact-to-cell plate alignment easier. Specification, p. 12, ¶ [0067].

Although some embodiments have been described above, it is noted that other embodiments are within the scope of the following claims.

VI. ISSUES

A. Are Claims 1-5, 11-15, 17, 18, And 20-25 Obvious Over The Asserted Combination of Aoki and Chu?

B. Are Claims 6-10 And 16 Obvious Over The Asserted Combination Of Aoki and Chu?

VII. GROUPING OF THE CLAIMS

Group 1: Claims 1-5, 11-15, 17, 18, and 20-25.

Group 2: Claims 6-10 and 16.

Within each group, the claims stand and fall together.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Are Claims 1-5, 11-15, 17, 18, And 20-25 Obvious Over The Asserted Combination of Aoki and Chu?

All claims were finally rejected over the asserted combination of Aoki and Chu. Claim 1 recites memory cells each having an area of about $6F^2$, sense amplifiers, bit lines coupled to the sense amplifiers in a folded bit liner configuration, with each bit line including a first level portion and a second level portion, and active area lines in which transistors are formed to electrically couple corresponding memory cells to corresponding first level bit lines.

As stated by the MPEP, a basic requirement of a *prima facie* case of obviousness is that the prior art *must* suggest the desirability of the claimed invention. The prior art clearly does not suggest the desirability of the claimed invention. In fact, Aoki teaches away from achieving $6F^2$ memory cell size with a folded bit line configuration. Aoki criticizes folded bit line arrangements as being space inefficient. Aoki notes that "the layout of the conventional open bit line configuration has an advantage over the folded bit line configuration in that the cell area can be reduced to 75%." Aoki, 2:14-16. Thus, a stated object of the "invention" of Aoki is "to provide a dynamic semiconductor memory device having an improved layout of open bit line configuration." *Id.*, 2:25-27. Significantly, Aoki expressly considered the possibility of both folded and open bit line configurations in its Background section, but Aoki discarded the idea of a folded bit line arrangement because of its space inefficiency. Thus, Aoki teaches away from

the claimed invention by suggesting that a $6F^2$ cell size cannot be achieved using a folded bit line arrangement.

Because Aoki teaches away from the claimed invention, there can be no motivation or suggestion to combine the teachings of Aoki with Chu to achieve the claimed invention.

Even if teachings of Aoki do not rise to the level of teaching away from the claimed invention, Aoki is objective proof that a person of ordinary skill in the art, prior to the invention of the present application, did not recognize that a $6F^2$ memory cell can be achieved with a folded bit line arrangement. This is a strong indication that there is no motivation or suggestion to modify Aoki by combining the teachings of Aoki and Chu in the manner proposed by the Examiner.

Because no motivation or suggestion existed to combine Aoki and Chu, the Examiner has failed to establish a *prima facie* case of obviousness.

Moreover, Chu does not provide any teaching or suggestion of the claimed invention. Chu proposes an architecture having an open bit-line cross-point memory cell layout that electrically behaves as a folded bit-line structure. However, there is no suggestion whatsoever that its layout can achieve the $6F^2$ memory cell area. Thus, there is no teaching in Chu that its structure can achieve the memory cell size recited in claim 1. Therefore, even if Aoki and Chu can be properly combined, the hypothetical combination of Aoki and Chu fails to teach or suggest each and every element of the claimed invention. A *prima facie* case of obviousness has not been established for this additional reason.

Independent claims 11 and 18 are allowable over the asserted combination of Aoki and Chu for similar reasons. For the foregoing reasons, the final rejections of claims 1-5, 11-15, 17, 18, and 20-25 should be reversed.

B. Are Claims 6-10 And 16 Obvious Over The Asserted Combination Of Aoki and Chu?

Claim 6 depends from claim 1, and is patentable over the asserted combination of Aoki and Chu for at least the same reasons as discussed above. Moreover, claim 6 recites further subject matter that is not taught or suggested by the hypothetical combination of Aoki and Chu. Claim 6 recites bit lines that extend generally along a same direction as active area lines, with the bit lines *intersecting the active area lines* at slanted portions. Claim 6 further recites contacts between bit lines and active area lines formed in the slanted portions.

Thus, claim 6 recites the following combination of elements: memory cells each having an area of about $6F^2$; bit lines coupled to sense amplifiers in a folded bit line configuration; and bit lines intersecting active area lines and slanted portions, with contacts formed in the slanted portions.

As noted above, Aoki does not teach or suggest the subject of claim 6. Moreover, Chu fails to teach or suggest bit lines intersecting active area lines, and contacts between bit lines and active area lines formed in the slanted portions, as recited in claim 6. Therefore, the hypothetical combination of Aoki and Chu does not teach or suggest these claim elements.

Claim 16 depends from claim 11, and is allowable over the asserted combination of Aoki and Chu for at least the same reasons. Moreover, there is no teaching by either Aoki or Chu of bit lines, coupled in a folded bit line arrangement, that intersect active area lines at slanted portions. Thus, even if the combination of Aoki and Chu is proper, the hypothetical combination of Aoki and Chu does not teach or suggest the elements of claim 16.

In view of the foregoing, it is respectfully requested that the final rejections of claims 6-10 and 16 be reversed.

IX. CONCLUSION

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

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CLAIMS ON APPEAL

1. A semiconductor device, comprising:

memory cells each having an area of about $6F^2$;

sense amplifiers;

bit lines coupled to the sense amplifiers in a folded bit line configuration, each bit line including a first level portion and a second level portion; and

active area lines, transistors being formed in the active area lines and electrically coupling corresponding memory cells to corresponding first level bit lines.

2. The semiconductor device of claim 1, wherein each pair of bit lines is vertically twisted at one or more predetermined locations, the bit lines in the pair transitioning between the first level portion and the second level portion at each twist.

3. The semiconductor device of claim 2, wherein a column pitch of each memory cell is 2F.

4. The semiconductor device of claim 1, wherein each memory cell includes a capacitor formed over the first level portion of each bit line.

5. The semiconductor device of claim 4, wherein the second level portion of each bit line is formed over each capacitor.

6. The semiconductor device of claim 1, wherein the bit lines extend generally along the same direction as the active area lines, the bit lines intersecting the active area lines at slanted portions,

the semiconductor device further comprising contacts between the bit lines and active area lines formed in the slanted portions.

7. The semiconductor device of claim 6, wherein the active area lines are generally straight and the bit lines extend in a wavy pattern.

8. The semiconductor device of claim 6, wherein the bit lines are generally straight and the active area lines extend in a wavy pattern.

9. The semiconductor device of claim 6, each bit line having a first portion on a first side of a corresponding active area line, a second portion on a second side of the corresponding active area line, and a third portion on the first side of the active area line.

10. The semiconductor device of claim 6, wherein the bit lines extend along generally the same direction as the active area lines so that the bit lines and active area lines intersect at predetermined locations.

11. A memory device comprising:

memory cells each having an area of about $6F^2$;

sense amplifiers;

bit lines coupled to the sense amplifiers in a folded bit line arrangement;

active area lines; and

transistors formed in the active area lines and electrically coupling corresponding memory cells to corresponding bit lines.

12. The memory device of claim 11, wherein each bit line has a first level portion and a second level portion, each transistor electrically coupling a corresponding memory cell to a first level portion of a corresponding bit line.

13. The memory device of claim 12, wherein each pair of bit lines is vertically twisted at one or more predetermined locations, the bit lines in the pair transitioning between the first level portion and the second level portion at each twist.

14. The memory device of claim 12, wherein each memory cell includes a capacitor formed over the first level portion of each bit line.

15. The memory device of claim 14, wherein the second level portion of each bit line is formed over each capacitor.

16. The memory device of claim 11, wherein the bit lines extend generally along the same direction as the active area lines, the bit lines intersecting the active area lines at slanted portions.

17. The memory device of claim 11, wherein each pair of bit lines is coupled to one side of a corresponding sense amplifier.

18. A method of making a memory device, comprising:

forming memory cells each having an area of about $6F^2$;

forming sense amplifiers;

coupling bit lines to the sense amplifiers in a folded bit line arrangement;

forming transistors in active area lines; and

the transistors electrically coupling corresponding memory cells to corresponding bit lines.

19. A method of making a memory device, comprising:

forming memory cells each having an area of about $6F^2$;

forming sense amplifiers;

coupling bit lines to the sense amplifiers in a folded bit line arrangement;

forming transistors in active area lines;

the transistors electrically coupling corresponding memory cells to corresponding bit lines;

forming each bit line of a first level portion and a second level portion; and

coupling each transistor to the first level portion of the corresponding bit line.

20. The method of claim 19, further comprising:

vertically twisting each pair of bit lines at one or more predetermined locations; and

transitioning the bit lines in the pair between the first level portion and the second level portion at each twist.

21. The method of claim 20, further comprising forming a capacitor of each memory cell over the first level portion of each bit line.

22. The method of claim 21, further comprising forming the second level portion of each bit line over the capacitor.

23. The semiconductor device of claim 1, wherein in the folded bit line arrangement a pair of bit lines is coupled to a same side of each corresponding sense amplifier.

24. The memory device of claim 11, wherein in the folded bit line arrangement a pair of bit lines is coupled to a same side of each corresponding sense amplifier.

25. The method of claim 18, wherein coupling the bit lines to the sense amplifiers in the folded bit line arrangement comprises coupling each pair of bit lines to a same side of each corresponding sense amplifier.